

**REMARKS**

As a result of the outstanding Office Action, claims 1-10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Jungerman et al ("Jungerman" – U.S. Patent No. 7,206,340) in view of Soma et al ("Soma" – U.S. Patent No. 6,775,321). Applicants respectfully traverse.

Applicants' claimed invention is a method and apparatus for clock signal recovery and for jitter measurement relative to the recovered clock signal by simulating a phase lock loop circuit that receives an external clock and external data signals, the recovered clock signal being recovered from the external clock. The external clock is acquired and stored as time domain data, from which edges of the external clock are detected. The edge time domain data is converted into the frequency domain to form frequency domain data which is multiplied by respective predetermined coefficients in different frequency domains, the coefficients simulating the filter response of the phase lock loop circuit. The resulting filtered frequency domain data is then converted back to the time domain to obtain the edges for the recovered clock signal. The time domain edge data for the recovered clock signal is compared with the time domain edge data for the external clock to measure the jitter of the external clock relative to the recovered clock signal.

Jungerman discloses a method of characterizing jitter of repetitive patterns at the output of a device under test that uses a pattern trigger from a pattern generator of the repetitive pattern or from a clock signal using a divider, the clock signal being either recovered from the repetitive pattern or provided separately. A designated edge at the beginning of the repetitive pattern is sampled and the slope of the edge determined. A set of amplitude values are acquired at the different occurrences of the designated edge. The set of amplitude values is converted to the frequency domain, and identified peaks in the frequency domain are truncated. An RMS value is extracted and converted, based upon the slope of the designated edge, to a corresponding RMS time jitter.

Applicants recite, in claims 1 and 7, a method and an apparatus for recovering a recovered clock signal from an external clock signal by simulating a phase locked loop. Jungerman does not indicate how the external clock is recovered from the repetitive pattern, and the pattern trigger derived from the external clock is not a recovered clock signal and no phase locked loop circuit is

shown in Jungerman. Applicants recite digitizing the external clock signal and storing the resulting time domain data in memory, i.e., acquiring time domain data from the external clock signal. Jungerman does not acquire time domain data from the external clock signal, but rather acquires time domain data from the repetitive data, i.e., the external data signal. Applicants then recite detecting the edges of the external clock signal from the time domain data. Since Jungerman does not acquire the external clock signal, Jungerman cannot detect the edges of the external clock signal, but rather acquires amplitude data at each designated edge as determined by the pattern trigger.

Next, Applicants recite converting the external clock edge time domain data into the frequency domain, whereas Jungerman converts acquired amplitude data from the designated edges of the repetitive pattern into the frequency domain. Subsequently Applicants recite multiplying the frequency domain data by respective predetermined coefficients, which claim 2 indicates are selected to simulate a filter corresponding to the phase lock loop circuit. Jungerman does not multiply any frequency domain data by coefficients, but rather truncates the peaks of the frequency domain amplitude data.

Finally, Applicants recite restoring the frequency domain data to the time domain data to obtain the edges of the recovered clock signal. Jungerman does not disclose a clock recovery system using a phase lock loop circuit, so Jungerman does not convert the frequency domain data to the time domain to obtain the recovered clock signal edges, but rather takes an RMS measurement in the frequency domain and converts that measurement in to an RMS measurement of the jitter in the time domain.

Therefore, Jungerman neither teaches nor suggests any of the steps or means recited by Applicants in claims 1 and 7. Since Jungerman is the primary reference cited by the Examiner, and Soma is cited only for the purpose of multiplying frequency domain data with coefficients in different frequency domains, the combination of Soma with Jungerman also does not teach or suggest the invention as recited by Applicants. Thus, claims 1 and 7 together with claims 2 and 8-10 dependent therefrom are deemed to be allowable as being nonobvious to one of ordinary skill in the art over Jungerman in view of Soma.

Claims 3 and 5 recite in similar language the same elements as in claims 1 and 7 with the further recitation of additional features. Since Jungerman in combination with Soma is does not to teach, show, or suggest the elements as recited in claims 1 and 7, claims 3 and 5 together with claims 4 and 6 dependent therefrom, also are deemed to be nonobvious to one of ordinary skill in the art over Jungerman in view of Soma.

In view of the foregoing, Applicant submits that the rejection has been overcome, respectfully requests that the rejection of claims 1-10 under 35 U.S.C. 103(a) be withdrawn and urges the allowance of claims 1-10, and such action and the issuance of this case are respectfully requested.

Respectfully submitted,

KATSUHIRO WATANABE, ET AL.

By /TFL Reg. No. 32152/  
Thomas F. Lenihan, Reg. No. 32,152  
Attorney for Applicant

TEKTRONIX, INC.  
Thomas F. Lenihan  
P.O. Box 500 (50-LAW)  
Beaverton, OR 97077  
(503) 627-7266

Attorney's Docket No.: 7651-US0      November 13, 2007